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Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components

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Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components

Introduction

The present solid state component level qualification procedures do not always ensure that the packaged component will operate reliably after assembly on printed wire boards (PWBs), or the like, since the free standing device level qualification may not induce the same thermomechanical stresses present in the post second level assembly state. As component interconnections decrease in size, e.g., the component is closer to the PWB; the interaction of the second level assembly becomes increasingly more likely on the component's performance. This document demonstrates how to evaluate the effect of assembly level operations and structures on components. As such, this document pertains predominantly to the following set of solid state devices and component packages that are described in the Scope. Knowledge of and comparison with packaged component failure mechanisms and modes is needed between the free standing and the assembled state. To ensure an effective qualification methodology for this set of solid state surface-mounted components, testing shall be performed in both the free standing and assembled state, including attached heat sinks where applicable. It should be noted that peripheral leaded surface-mount components are not considered in this document because, in general, the thermomechanical stresses imparted to the component in its assembled state are minimal, due to the inherent flexibility of their leads.

Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components

(From JEDEC Board Ballot, JCB-05-56, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication contains a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products, in particular leadless chip carriers, ball grid array (BGA) packages, direct chip attach die and packages with exposed pads that are attached to the PWB for thermal considerations. Assembly level testing may not be a prerequisite for device qualification; however, if the effect of assembly conditions on the component is not known, there could be reliability concerns for that component that are not evident in component level testing. As such, it is recommended that assembly level testing be performed to determine if there are any adverse effects on that component due to its assembly to a PWB.

These reliability stress tests have been found capable of stimulating and precipitating failures in assembled components in an accelerated manner, but these tests should not be used indiscriminately. Each qualification should be examined for:

a) Any potential new and unique failure mechanisms.

b) Any situation where these tests and/or conditions may induce false failures.

In either case the set of reliability requirements, tests and/or conditions should be appropriately modified to properly comprehend the new situations.

This document does not relieve the supplier of the responsibility to meet internal or customer specified qualification programs.

2 Terms and definitions

second level assembly: The attachment of a component to the next level of assembly packaging.

packaged device: A semiconductor device within an enclosure that allows electrical connection to and provides mechanical and environmental protection for that device.

free-standing state (of a component): The state of a component that is not attached to the next level of assembly packaging.

assembled state (of a component): The state of a component that has been attached to a second level assembly.

2 Terms and definitions (cont'd)

chip package interaction (CPI): The interaction between the semiconductor package stresses and the semiconductor device.

peripheral-leaded surface-mount component: A component with a metal frame that provides external surface-mountable terminals located around the periphery of the body of the component.

3 Reference Documents

JEP122, *"Failure Mechanisms and Models for Silicon Semiconductor Devices"*

JESD74, *"Early Life Failure Rate Calculation Procedure for Electronic Components"*

JESD85, *"Calculation of Failure Rate in Units of FITs"*

JESD91, *"Method for Developing Acceleration Models for Electronic Component Failure Mechanisms"*

JESD94, *"Application Specific Qualification using Knowledge Based Test Methodology"*

JESD22, *"Reliability Test Methods for Packaged Devices"*

JEP131, *"Process Failure Modes and Effect Analysis (FMEA)"*

JESD47, *"Failure Mechanisms and Models for Silicon Semiconductor Devices"*

IPC/JEDEC 9702, *"Monotonic Bend Characterization of Board-Level Interconnects"*

IPC 9701, *"Solder Joint Reliability Test Method"*

SEMATECH White Paper #99083810A-XFR, *"Use Condition Based Reliability Evaluation of New Semiconductor Technologies"*

SEMATECH White Paper #99083813A-XFR, *"Use Condition Based Reliability Evaluation: An Example Applied to Ball Grid Array (BGA) Packages"*

4 Understanding stress interactions

The apparent stresses and distribution of stresses imparted to the solid state component during free-standing component qualification testing may not match the actual stresses and associated distribution that the component will be subjected to when surface mounted on a printed wiring board (PWB). Failure modes may also be different. Figure 1 shows the various interactions that exist between the packaged device and its free-standing and assembled state that can affect the component's reliability in the final field application.

Area 1 in Figure 1 refers to the reliability of the free-standing component prior to assembly to a PWB. Qualification procedures have been established for components, see JESD47 (Stress Test Driven Methodology) and JESD94 (Application Specific Qualification using Knowledge Based Test Methodology).

4 Understanding stress interactions (cont'd)

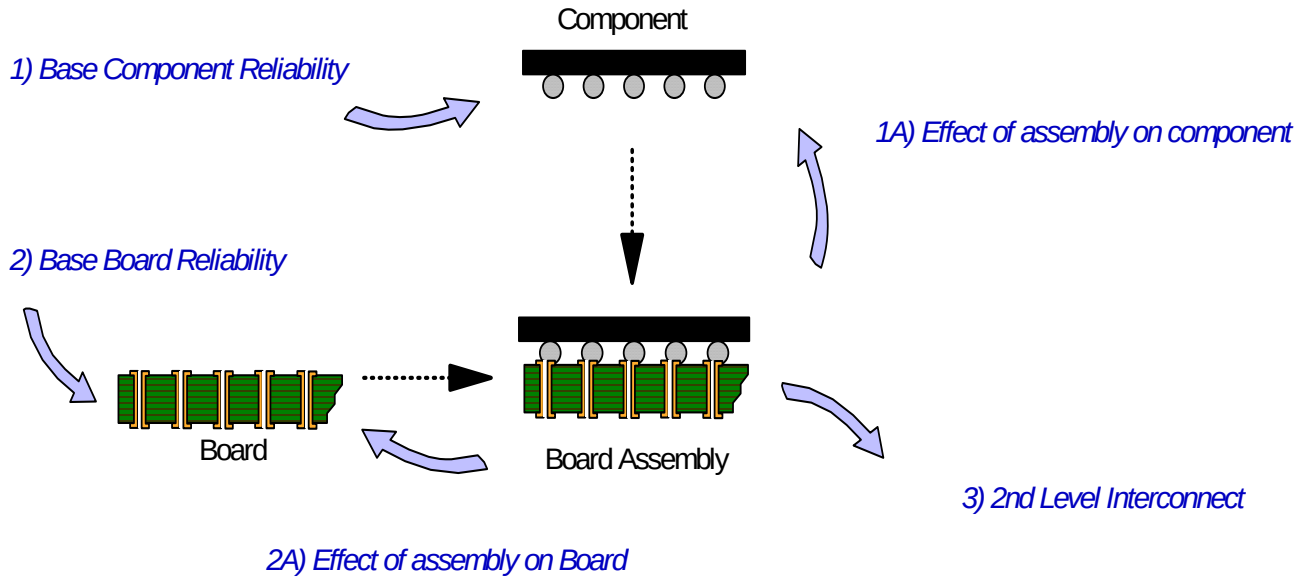

Figure 1 — Levels of Assembly - Interaction of packaging technical concerns

When the component is assembled onto a printed wiring board (PWB), or the like, the assembly process can affect the reliability of the component by exposing it to new or altered assembly related stress levels and stress distributions as shown in area 1A of Figure 1. This is the primary focus in this document. The major concern is that the component, as assembled, will exhibit failure modes that were not detected during the qualification of the free-standing component. Failures can be found in the various areas of the component including the package materials, package circuitry and the silicon device due to chip to package interactions.

Example: A specific example of this is beam lead failures seen in micro BGA packages. The micro BGA package typically uses a highly compliant and low modulus elastomer to de-couple the die from the flex tape. Failures are generally not seen during the component level qualification. However, when the package is assembled on the next level, there is a shift in the composite coefficient of thermal expansion (CTE) of the assembled component. This mismatch drives stresses from the solder joints to the copper beam leads inside the package. This may result in beam lead failures, which can be detected during thermal cycling tests of the assembled component.

Area 2 in Figure 1 refers to the reliability of the PWB. PWB stand-alone reliability testing is not addressed in this document.

Area 3 is the interconnection between the component and the PWB, also referred to as the second level interconnect. It will be addressed in this document, **only as it relates to the reliability of the component**, including its solder interconnection members, e. g., BGA, flip chip, or LCC solder joints. Items associated with the PWB and their affect on the PWB solder interconnection are **not** being covered in the assembly test sequence, including PWB surface contamination, insufficient cleaning of trapped fluxes or improper handling of the PWB assembly that cause PWB failure.

5 Determining second level test requirements

One should examine the suggested tests, failure mechanisms and failure modes associated with component level qualification and compare them to those associated with assembly level qualification. By examining the failure modes in the assembly level qualification, that are not detected during component level qualification, it is possible to specify the assembly level tests that should be used in conjunction with the component level tests. This will better ensure that the qualification procedure used can detect all known failure modes and mechanisms for a component in its projected use.

Each qualification project should be examined for (a) any potential new and unique failure mechanisms and (b) any situations where the standardized tests and conditions may induce failures not relevant in the field. Use of both historical knowledge information and failure modes and effect analysis (FMEA) is a means that can be used to improve the qualification process test sequence selection.

Annex A provides a fairly extensive list of various failure mechanisms for components in the free standing and assembled condition and it gives a brief description of their relationship to accelerated tests. Though extensive, this list should not be assumed to be complete. With new materials and processes, new failure mechanisms continue to be found. Annex A should help facilitate the process of identifying potential failure mechanisms and the determination of an appropriate qualification strategy and plan. It can be used in conjunction with Table 2 where the same failure mechanisms are listed with the corresponding reliability stress test(s) that can be used to reveal reliability problems.

6 Component level/ second level assembly qualification tests

Table 1 shows a comparison between the tests and conditions used to evaluate and qualify free-standing components versus the tests and conditions used to evaluate and qualify components assembled to PWB, or the like. It is only to be used as a general comparison between the testing performed on free-standing versus assembled components. It is not intended to be used as a list of required stresses. Dependent on the specific application, other tests or combination of tests may be appropriate. This must be evaluated on a case-by-case basis. Note that sequential and simultaneous environmental testing has been used where appropriate, per reference.

7 Comparison of qualification methodologies

A component and assembly level test selection guideline for the various reliability failure mechanisms, listed in Annex A, is provided in Table 2. The failure modes listed are typical, but with ever changing material sets, device construction and assembly conditions the list in Table 2 is not guaranteed to be complete and must be considered strictly as a guide. Tests performed at component and assembly level are designated “C” and “A”, respectively. Failure mechanisms that are found in both component and assembly level tests, but shift either in time to failure or location of failure, are denoted by “M” for a failure mode shift. Table 2 provides a reference as to which stress tests can be used to uncover the particular failure mechanism. It should be used as a guideline only.

7 Comparison of qualification methodologies (cont'd)

Table 1 — Typical JEDEC Stress Tests For Component & Assembly Level Testing

TEST #	TEST	COMPONENT LEVEL TESTING	BOARD ASSEMBLY LEVEL TESTING
1a	Preconditioning	JESD22A113, Appropriate MSL Level (including moisture soak) prior to TC, THB, HAST, HTS	Not Done
1b	Assembly of components on PWBs inc. Preconditioning	Not Done	JESD22A113 for the specific MSL level, with a minimum of three reflow cycles, dependent on the assembly time schedule.
2	Unbiased HAST	JESD22-A118: Conditions A (130 °C/ 85%RH) or B (110 °C / 85%RH)	Typically Not Done, but Optional for Readout Ease. PWB materials must be compatible with HAST test conditions. JESD22A110: Conditions A (130 °C/85%RH) or B (110 °C/85%RH)
3	High Temp Storage	JESD 22-A103: Typically Conditions A (125 °C) or B (150 °C)	Optional for Readout Ease Only If performed JESD22A103 Conditions A (125 °C) or B (150 °C)
4a	Temp Humidity Bias	JESD22A101 (85 °C/ 85%RH) with Bias	Typically 50 °C to 85 °C & 80% to 85 % RH with Bias
4b	Temp Humidity no Bias	JESD22A101 (85 °C/ 85%RH) without Bias	Typically 50 °C to 85 °C & 80% to 85 % RH without Bias
5	HAST with Bias	JESD22A110: Conditions A (130 °C/ 85%RH) or B (110 °C/ 85%RH)	Typically Not Done, but Optional for Readout Ease. PWB materials must be compatible with HAST test conditions. JESD22A110: Conditions A (130 °C/85%RH) or B (110 °C/ 85%RH)
6	Temp Cycling	JESD22A104: Typical Test Conditions B (-55 °C to 125 °C) or G (-40 °C to 125 °C)	JESD22A104: Recommended Test Condition J (0 °C to 100 °C) Application specific alternatives. Care should be taken if these alternative test conditions are used. Conditions are: G (-40 °C to 125 °C), K (0 °C to 125 °C) or L (-55 °C to 110 °C). Soak mode options: 2, 3 or 4
7	Power Temperature Cycling	JESD22A105: Condition A (-40 °C to 85 °C) or B (-40 °C to 125 °C) (*Typically on high power devices*)	JESD22A105: Conditions A (-40 °C to 85 °C) or B (-40 °C to 125 °C) (*Typically on high power devices*)
8	Mechanical Shock (Drop Test)	JESD22B104: Condition A (Peak acceleration 500G)	JESD22B110: Condition A (Peak acceleration 500G) & JESD22-B111
9	Vibration, Variable Frequency	JESD22B103: Condition 1 (Peak acceleration 20G)	JESD22B103: Condition 1 (Peak acceleration 20G)
10	Bending: Monotonic & Cyclic	Not Done	See IPC/JEDEC 9702
11	Solder Creep Rupture	Not Done	Done
12	Autoclave (SPP)	JESD22A102, (121 °C)	Not Done
13	Thermal Shock	JESD22A106, Condition C (-40 °C to 125 °C) *(Recommended for characterization & not generally used for qualification. Use only with technical justification)*	Not Done
14	Low Temperature Storage	JESD22A119	Not Done

Notes:
This is a compilation of typical stress tests. It is not intended to be used as a list of required stresses.
Stress tests selected should be based on potential failure mechanisms. Dependent on the failure mechanism of interest, a combination of tests, such as HALT, may be an applicable test strategy.

7 Comparison of qualification methodologies (cont'd)

Table 2 — Component and assembly level test selection guidelines for various reliability failure mechanisms

TESTS From TABLE 1 / Failure Mechanism	1a Precon	1b Assembly	2 UHAST	3 HTS	4a THB	4b TH	5 HAST	6 TC	7 PTC	8 Shock	9 Vibration	10 Bend	11 SCR	12 Autoclave	13 TS
THERMAL MECHANICAL															
SOLDER FATIGUE															
Flip Chip Underfill	C	A						CAM							
Flip Chip No Underfill	C	A						CA							
BGA Joints		A						A	A						
LCC Solder Joints		A						A							
SOLDER CREEP RUPTURE															
Heat Sink Assembly		A						A					A		
METAL FATIGUE															
Wire Bonds	C	A						CA							C
ILB/ OLB	C	A						CAM							C
μBGA Beam Leads	C	A						CA							C
PTHs	C	A						CAM	A						C
Circuit Lines	C	A						CAM	A						C
μVia Joints	C	A						CAM							
DELAMINATIION															
Device to Underfill	C	A	C		CAM	C	C	CA							
Device to Die Attach Adhesive	C		C		CAM	C	C	C							
Device to Glob Top/ OM	C	A	C		CAM	C	C	CA							
Substrate to Underfill	C	A	C		CAM	C	C	CA							C
Substrate/ Solder Mask	C	A	C	C	CAM	C	CAM	CAM							C
Substrate to Glob Top/ OM	C	A	C	C	CAM	C	C	C							C
Substrate IC Pads	C	A	C	C	CAM	C		CAM							C
Substrate Circuit Lines	C		C	C	CAM	C		C							C
WB/I/OLB/ to Glob Top/ OM	C	A	C	C	CAM	C		C							C
Cap/ Stiffener to Attach Adhesive	C	A	C	C	CAM	C	C	CAM							C
Cap/ Stiffener to HS Adhesive	C	A	C	C	CAM	C		CAM							
Chip/ Package Interact		A	C	C	A	C		A							
CRACKING/ MICROCRACKING															
Device	C	A						CAM							C
Thin Film Passivation	C							CA							C
Solder Mask	C	A						CAM	C						C
Circuit Lines	C	A						CAM	C						C
Underfill	C							CA							C
DEFECTS: ASM/ REWORK INDUCED															
BGA Voids		A						A	A						
BGA Fillet Geometry		A						A	A						
Non-Wets (BGA & Flip Chip)	C	A						CAM	A						C
Cu Dissolution PTH Rim/Pads	C							C							C

7 Comparison of qualification methodologies (cont'd)

Table 2 — Component and assembly level test selection guidelines for various reliability failure mechanisms (cont'd)

TESTS From TABLE 1 / Failure Mechanism	1a Precon	1b Assembly	2 UHAST	3 HTS	4a THB	4b TH	5 HAST	6 TC	7 PTC	8 Shock	9 Vibration	10 Bend	11 SCR	12 Autoclave	13 TS
WB/ILB/OLB DEFECTS															
Nicks	C							C							C
Poor Bond Foot	C							C							C
Surface Finish	C							C							C
CIRCUIT LINE DEFECTS															
Neck Downs	C							C							C
Mouse Bites	C							C							C
PTH DEFECTS															
Plating Discontinuous	C							C							C
Rim Voids	C							C							C
CORROSION/ MIGRATION MECHANISMS															
CONTAMINATION															
Handling	C	A	C	C	CAM	C	CAM								
Trapped Residues: Component Assembly	C		C	C	C	C	C								
Substrate Mfg Operations	C		C	C	C	C	C								
GALVANIC/ ELECTROYTIC CELLS															
Mixed Metal Interfaces	C		C	C	C	C	C	C						C	
Process Residues	C		C	C	C	C	C							C	
OXIDATION															
Oxide Film Growth	C		C	C	C	C									
DELAMINATION															
Interfacial Corrosion	C	A	C	C	CAM	C	CAM	CAM						C	
THERMAL AGING MECHANISMS															
MATERIAL BREAKDOWN															
Oxidation	C			C											
Electrical	C			C											
Thermal Breakdown	C	A		CAM				A							
Intermetallic Breakdown	C	A		CAM				A		A	A	A			A
MECHANICAL STRESS MECHANISMS															
Handling		A									CAM	A			
Bending: Monotonic		A										A			
Bending: Cyclic		A										A			
Dropping		A								CAM					
Vibration		A									CAM				

C = Test done at component level to observe specific failure mechanism in the component.
A = Test done at assembly level to observe specific failure mechanism in the component.
M = Different failure mode observed between component and assembly level tests for the same failure mechanism in the component.

8 General requirements

8.1 Test samples

8.1.1 Lot requirements

To assess manufacturing variability and its impact on reliability, the component test samples should be comprised of approximately equal numbers from three (3) nonconsecutive component lots to evaluate variability from the component qualification family. Other appropriate means may be used with justification.

8.1.2 Production requirements

All test samples shall be fabricated and assembled to the PWB, or the like, in an industry standard manner that is recommended by the supplier for such component. For these test samples, preconditioning of the component should be preformed per JEDS22-A113, which includes a total of at least three reflows with one of the reflows used for the actual assembly of the test sample component(s) to the PWB, or the like. It should be noted which of the reflow cycles was used as the assembly step to the PWB. As with standard component preconditioning, the reflows should reflect the solder regimen being used in the actual application.

8.1.3 Test hardware

The test panel, if possible, should reflect the projected end-use assembly structure/ layout, material set and construction. If several end-uses are anticipated, the worst case PWB structure should be used based on the test being performed. Worst case should be determined by way of modeling simulations of the component and the PWB. If the structure for the end-use is not known, then use of a test vehicle such as that described in JESD22-B111, IPC/JEDEC 9702 or IPC 9701, is acceptable. The test vehicle selected should most closely approximate the expected end-use assembly structure.

The assembled test vehicle structure (test card and test device) should to be designed for test compatibility. Typically a mating daisy chain structure for the component and the PWB is used. Upon assembly, the meshed daisy chain structures allow testing of the component and its interface to the PWB. The daisy chains should typically be on the top surface of the PWB to insure test vehicle robustness. Other configurations can be used if the PWB traces are susceptible to damage from the test being performed, e.g., anvil abrasions associated with bend testing. For long term testing, especially in temperature cycling, test boards that have daisy chains integrated into their structure, including the plated through holes, typically become the weakest link and fail earlier than desired thus making the test vehicle untestable for component level failures. Full test coverage of the solder joints of interest is preferred. Care must be taken, though, not to have daisy chains that are too long. If too long, the resistance of the chain will be high and as such failures are more difficult to detect and ultimately isolate. Employment of functional components is also acceptable and can be provide insight into actual product performance, if proper care it taken in the test vehicle design. If improperly designed, the functional device parameters could mask test failures by lack of test sensitivity. In general, the devices used for reliability investigations should be chosen according to the following criteria: 1- relevancy for the intended use, 2- ease of analysis and 3- dominant failure mechanism to be investigated under the planned stress condition.

8.1 Test samples (cont'd)

8.1.4 Documentation

Details of the test set-up and results should be reported, as specified in applicable procurement documents.

9 Test criteria

9.1 Procedure

Once the test hardware is assembled and prepared for testing, appropriate test procedures should be followed for the stress test being performed. Test performance can be tracked by both discrete interval measurements or by in-situ continuous monitoring. Appropriate tester setups should be followed, with care taken to guarantee that the test interval, tester accuracy and tester setup meet appropriate industry standards. If in-situ continuous monitoring is not used, a test method capable of resolving a low resistance change in each pin loop pair is necessary, such as the four-point probe methodology. With in-situ interval testing, the resistance change criteria used can be critical in the timely discovery of test fails. Failure criteria need to be set to the specific application. As a general rule of thumb a 20% change in electrical resistance represents a test failure in each test loop. If the test method selected is not capable of resolving this level of resistance shift then there is the likelihood that tests failures will not be detected in a timely manner, thus affecting any failure models or statistics being formulated. If a bench top discrete measurement technique is used, the test interval readout schedule should be determined based on the failure mechanisms of interest. Generally readouts are made more often in the early portion of the reliability test sequence in order to capture early test fails or test setup problems.

10 Failure Analysis

Failure analysis is used to verify the location and mechanism of the failure. The most important aspect of failure analysis is the verification that the failure is associated with the component and not the PWB. Also it must be determined that it would be the type of failure that is relevant to application conditions and situations. As such it is important to isolate the failure and assure that it is associated with the component and not the test setup, including the tester, cabling or the PWB on which the component of interest has been assembled. Care must be taken during failure analysis not to disturb the failure. In particular, if the component needs to be removed form the PWB, extreme care must be taken. It is preferred to do the failure analysis on the assembly, if possible.

Non-destructive failure analysis tools can also be used. They include coupled scanning acoustic microscopy (CSAM), x-ray, time domain reflectometry (TDR), and side view optical microscopy. Common methods used in destructive failure analysis include, but are not limited to, cross section, dye penetrant, scanning electron microscopy (SEM) and energy dispersive x-ray (EDX).

ANNEX A Possible Component Failure Mechanisms

FAILURE MECHANISM	COMMENTS
I. THERMAL MECHANICAL MECHANISMS	Thermal mechanical failure mechanisms are those associated with changes in temperature and the effect this has on the component and its assembly to a PWB, or the like. Generally differences in material properties between structures, such as CTE, Young's modulus, Poisson ratio, either within the component or the associated assembly causes problems as the component experiences different temperatures in its use condition. Some failure mechanisms, such as delamination can occur as the result of thermal mechanical and moisture driven events.
1 - SOLDER FATIGUE	
A - FLIP CHIP (C4) JOINTS WITH UNDERFILL	Solder fatigue can occur in the encapsulated state. Though typically associated with delamination of the underfill, it can occur without loss of underfill adhesion. There can be shifts in failure sites between component and assembly level reliability testing.
B - FLIP CHIP (C4) JOINTS NO UNDERFILL	Unencapsulated flip chip joints are rarely used. Joint life is severely diminished without an appropriate underfill around them. Failure is easily seen at component level test and is associated with the distance from neutral point (DNP) of the flip chip joints.
C - BGA JOINTS	BGA life is affected by a wide range of attributes. It can only be observed after assembly. Key reliability factors: 1- BGA pad dimension, shape, metallurgy, configuration and cross section (captured or non-captured) ; 2- Ball size, standoff and composition; 3- PWB thickness, x-section, CTE (X, Y, Z), warpage and PTH pattern; 4- Assembly configuration, including near neighbor components, single versus double sided (with shared via) and heat sink size and attachment method; and 5- Assembly attributes including paste volume, flux type, assembly profile, rework method, profile and reflow atmosphere. The module factors, such as device size, device type (wire bond or C4), chip outline with respect to BGA pads and module material properties also affect assembly BGA interconnection reliability.
D - SURFACE-MOUNT LCC SOLDER JOINTS	Solder fatigue of LCC solder joints is a common concern. Due to the stiffness of the LCC and the minimal size and height of the solder joint, solder fatigue often occurs relatively early.
2 - SOLDER CREEP RUPTURE	
A - HEAT SINK ATTACHED TO MODULE ASSEMBLY	Depends on heat sink size, attachment method and position of the heat sinked module in the field (gravity effect). Addition of a heat sink to a component affects the stiffness of the assembly and therefore influences product reliability.
3 - METAL FATIGUE	
A - WIRE BONDS	Problems with wire bonds are readily found at component level test.
B - INNER/ OUTER LEAD BONDS (ILB/ OLB)	Problems with ILB/ OLB joints are readily found at component level test. There can also be a shift of failure modes during assembly level test.

ANNEX A Possible Component Failure Mechanisms (cont'd)

C - MICRO BGA BEAM LEADS	Problems with micro BGA beam leads can be found at component level test, but are also detectable at assembly level test. There does not seem to be a shift in failure location between the component and second level testing.
D - PLATED THROUGH HOLES (PTH)	PTHs in both the component and PWB can be affected by component assembly. Dependent on the substrate size, interconnect location and type and device location, especially for flip chip modules, the PTHs can be stressed and crack, predominately at the barrel to surface interface.
E - CIRCUIT LINES	Dependent on stress risers, circuit lines can be stressed and crack. This is observed in both component and assembly level tests. Dependent on stress location, failure locations can shift between the two sets of tests.
F - MICROVIA JOINTS	Microvia joints can fail due to poor interconnection to lower levels of metallurgy or due to external forces such as heat sink loading.
4 - DELAMINATION	
Delamination is triggered by insufficient interfacial strength between two adjacent materials. This strength is determined by the following factors: 1) chemical bonding (covalent binding), 2) physical adsorption (Lipshitz-vanderWaal forces) and 3) mechanical interlocking (related to surface roughness). Interfacial strength can be decreased by the influence of moisture and temperature. If, at any test condition the stresses applied at the interface increases the strength of it, delamination will occur.	
A - DEVICE	
A1 - UNDERFILL	Underfill delamination next to the device can be detected in component level tests. Once delamination occurs, the flip chip solder joints fail soon thereafter.
A2 - DIE ATTACH ADHESIVE	Die attach adhesion can be detected in component level test.
A3 - OVERMOLD/ GLOB TOP	Overmold / glob top adhesion loss can be detected in component level test.
B - SUBSTRATE	
B1 - UNDERFILL	Underfill delamination at the substrate can be detected in component level tests.
B2 - SOLDER MASK	Solder mask cracking can occur in both component and assembly level tests. The severity of the cracking is substantially diminished in second level tests since thermal cycle conditions used are typically less severe and more closely aligned to application requirements. The material properties of solder mask materials, including t_g, usually do not withstand extended testing at component level test temperature extremes.
B3 - OVERMOLD/ GLOB TOP	Overmold/ glob top cracking can be observed at component level test.
B4 - INTERCONNECT PADS	Interconnect pad delamination can be seen in both component and second level tests. Dependent on the assembly, including heat sink, this can occur in different regions and at different points in time for component versus second level testing.
B5 - CIRCUIT LINES	Circuit line delamination can be observed in component level testing.
C - WB/ ILB/ OLB	
C1 - OVERMOLD/ GLOB TOP	Overmold/ glob top delamination can be observed in component level test.

ANNEX A Possible Component Failure Mechanisms (cont'd)

D - CAP/ STIFFENER	
D1 - ATTACH ADHESIVE	Delamination of cap and stiffener adhesive joints can be observed in both component and assembly level tests. The effect of a heat sink on that bond line can only be observed in the assembled mode.
D2 - HEAT SINK ADHESIVE	Delamination of the heat sink adhesive can only be observed in the assembly level tests, since the heat sink is attached during the second level assembly operation.
E - CHIP PACKAGE INTERACTION (CPI)	Delamination of low k dielectric material in the device due to stresses from the package. It can be found in component testing, especially if component is preconditioned prior to test. Problem is exacerbated in assembly testing due to added stresses and assembly temperature exposure.
F - THERMAL PAD/ OVERMOLD DELAMINATION	Delamination of the overmold from the thermal pad due to the heat from the operating device.
5 - CRACKING/ MICROCRACKING	
A – DEVICE	Device cracking can be observed at component level test. In the case of flip chip devices, if the device does not crack during either a few temperature cycles or during second level assembly of the component, it won't occur at a later time.
B - DEVICE THIN FILM PASSIVATION	Device passivation cracking can be detected as the result of component level test.
C - SOLDER MASK	Solder mask cracking will be more severe in component level tests. Second level testing should be performed to determine if the cracks are a concern for the specific application.
D - CIRCUIT LINES	Circuit line cracking can be observed in both component and second level tests. Dependent on the test conditions used, this can be eliminated. Application conditions should be considered when evaluating the factors contributing to this failure mode.
E - UNDERFILL	Cracking of the underfill can be observed in component level tests.
F - HEAT SINK ATTACH TO BARE DIE	Cracking of the die due to the heat sink attach process. This can be due to excessive force during the attach process or entrapped particulates between the die and heat sink or previously damaged die.
6- DEFECTS	
A - ASSEMBLY/ REWORK INDUCED	
A1 - BGA VOIDS	The effect of BGA voids on reliability can only be tested at assembly level. The level of voids is related to solder composition, reflow profile and flux used.
A2 - BGA FILLET GEOMETRY	The effect of BGA fillet geometry on reliability can only be tested at the assembly level. Assembly profiles and assembly warpage factors can dramatically affect the end results.
A3- NON-WETS (BGA & C4)	The effect of BGA non-wets can only be observed in the assembly level tests. C4 non-wets can be found in both component and assembly level tests.
B - WIRE BOND	
B1 – NICKS	This can be found in component level test.
B2 - SQUISHED BOND FOOT	This can be found in component level test.
B3 - SURFACE FINISH	This can be found in component level test.

ANNEX A Possible Component Failure Mechanisms (cont'd)

C - ILB	
C1 - NICKS	This can be found in component level test.
D - CIRCUIT LINE	
D1 - NECK DOWNS	This can be found in component level test.
D2 - MOUSE BITES	This can be found in component level test.
E - PTH	
E1 - PLATING DISCONTINUITIES	This can be found in component level test.
E2 - RIM VOIDS	This can be found in component level test.
II. CORROSION/ MIGRATION MECHANISMS	Corrosion/ migration failure mechanisms are those associated with the destruction of a metal by chemical or electrochemical action. Such failure mechanisms need a moisture path, surface contamination and for metal migration to occur, a bias voltage. Moisture paths are most commonly caused by assembly operations, cracks, delamination, and pinholes in passivation or poor step coverage. The rate of corrosion processes is accelerated by moisture, temperature, voltage, contamination, conductor spacing and material properties.
1 - CONTAMINATION	
A - HANDLING	Handling is always an issue. It is best to process parts through the full range on operations, including assembly to identify any areas of concern.
B - TRAPPED RESIDUES	
B1 - MODULE ASSEMBLY	Flux residues are always a concern. Problems can be identified in component level test.
B2 - CARRIER MFG OPERATIONS	Residual contaminants from carrier processing can be a concern. Problems can be found in component level test.
2 - GALVANIC CELLS	
A - BILL OF MATERIAL S	Problems associated with incompatible materials in a structure, i.e. formation of unacceptable galvanic cells, can be found at component level test.
B - PROCESS RESIDUES	Process residue problems can be found in both component and assembly level test.
3 - OXIDATION	
A - OXIDE FILM GROWTH	Oxide film growth can be found at component level test.
4 - DELAMINATION	
A - LOSS OF INTERFACIAL ADHESION	Delamination is triggered by insufficient interfacial strength between two adjacent materials. This strength is determined by the following factors: 1) chemical bonding (covalent binding), 2) physical adsorption (Lipshitz- vanderWaal forces) and 3) mechanical interlocking (related to surface roughness). Interfacial strength can be decreased by the influence of moisture and temperature. If, at any test condition the stresses applied at the interface increases the strength of it, delamination will occur. Loss of interfacial adhesion can be found in both component and assembly level test. The failures may be exacerbated by the component being subjected to assembly operations where contaminants can speed the growth of dendrites.

ANNEX A Possible Component Failure Mechanisms (cont'd)

III. THERMAL AGING MECHANISMS	Thermal aging mechanisms are those associated with high temperature. They usually involve degradation of a material set associated with the component. It can result form long term application of temperature, such as in the field application, or from the assembly of the component at elevated temperatures where component material set degrades.
1- MATERIAL BREAKDOWN	
A- MATERIAL OXIDATION	Material oxidation can be found in both component and assembly level test. Assembly conditions can exacerbate the condition.
B - ELECTRICAL DEGRADATION	This can be found in component level test.
C - THERMAL DEGRADATION	Thermal degradation can be found in both component and assembly level test. Assembly conditions can exacerbate the condition
D - INTERMETALLIC DEGRADATION	This can be found in component level test.
IV. MECHANICAL STRESS MECHANISMS	Mechanical stress failure mechanisms are those associated with the handling, mishandling, assembly, test and vibration of a component and its assembly. This can occur in the assembly, shipment and actual use of the component.
1 - HANDLING	This is found at component and assembly level testing. Various manufacturing operations, such as insertion and removal from test fixtures, can affect the component and its assembly
2 - BENDING - MONOTONIC	This is found at assembly level and is associated with flexure of a given component assembly, including insertion of neighbor components or daughter cards. Concerns such as component pad plating material, that can produce brittle intermetallics, are addressed in this.
3 - BENDING - CYCLIC	This is found after assembly operations or during shipment if improperly packed. It is often associated with in circuit test actuation, routing operations, or in use, such as key actuation on a hand held electronic device.
4 - DROPPING	This is found at both component and assembly level test and is associated with the mishandling of a component or its assembly.
5 - VIBRATION	This is found at component and assembly level can is associated with either use conditions, assembly operations such as routing operations or during shipment if improperly packed.
6 - COSMETIC DAMAGE	Areas of cosmetic damage include die cracks, package cracks, etc.

Annex B (informative) Differences between JEP150.01 and JEP150

This annex briefly describes most of the changes made to entries that appear in this publication, JEP150.01, compared to its predecessor, JEP150 (May 2005). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of change
3	Replaced reference JESD90 with JESD91, the number was incorrectly stated.

Standard Improvement Form

JEDEC JEP150.01

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

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The referenced clause number has proven to be:

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2. Recommendations for correction:

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